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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,242	08/30/2001	Wen Lin	00-LM-117	9379

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EXAMINER	
CHOI, WOO H	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,242	LIN, WEN	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *23-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 28-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-31* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/04/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1 – 22, and 28 - 31, drawn to a computer system with a mass storage device and a controller, classified in class 711, subclass 112.

   II. Claims 23 – 27, drawn to a disk mass storage device with a storage surface, a head and a storage controller, classified in class 360, subclass 75.

2. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because a mass storage device claimed in the combination is broadly claimed without requiring the specific limitations required in the subcombination. The subcombination has separate utility as a non-volatile peripheral storage device that can be used in any computing system.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Applicant's attorney of record, Mr. Stuart T. Langley on June 04, 2004, a provisional election was made without traverse to prosecute the invention of group I, claims 1 – 22 and 28 - 31. Affirmation of this election must be made by applicant in replying to this Office action. Claims 23 – 27 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Objections

5. Claims 19 – 22 are objected to because of the following informalities:

Change "The computing device of claim 1" to -- The computing system of claim 1 -- Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 18 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for elements of the claimed limitation separately, does not reasonably provide enablement for the combination of the all of the elements in one embodiment. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims.

Claim 18 requires that the mass storage device's interface be implemented by the servo controller and that it implements a physical interface to the data/control bus. Enabling disclosure

for the servo controller portion of the limitation can be found in figures 5, 6 and 7. However, figures 5 and 7 do not disclose a mass storage device interface with a physical interface to a data/control bus of the processor. Figure 6, which may show such a physical interface does not meet the requirements of claim 1. Figure 2 shows such a physical interface. However, this figure does not meet the requirements of the servo controller implementation of the interface.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 5 – 11 and 28 – 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanenbaum (Operating Systems, Design and Implementation, Prentice-Hall, 1987).

10. With respect to claims 1, 5, 6 and 11, Tanenbaum discloses a computing system (page 114, figure 3-3) comprising:

a processor (CPU) having a data/control bus interface;

a data/control bus (System bus) implementing one or more device communication channels;

a data memory (Memory) coupled to the processor;

a mass storage device (Drive) having an interface for communicating mass storage transactions; and

a controller (Disk controller with DMA) having a memory interface coupled to the data memory (interface to the system bus) and a mass storage interface (interface to the drive) coupled to the mass storage device's interface and operable to conduct mass storage transactions between the data memory and the mass storage device.

11. With respect to claims 7, 28 and 29, the system further comprising storage controller processes (page 92, disk task) and application behavior processes implemented using the processor (page 92, other task, for example, terminal, memory, clock, file system, and user programs).

12. With respect to claims 8, 9, and 30 the storage controller processes map storage requests generated by the application behavior processes expressed in logical geometry terms into storage requests expressed in physical geometry terms (page 118, 3.2.3. Device Drivers, given a request to read a block, block n for example, the device driver figures out where on the disk the requested block actually is, see also pages 482 – 484).

13. With respect to claim 10, the processor implements data structures storing physical geometry information about the mass storage device (pages 482 – 484).

14. With respect to claim 31, the storage related instructions include instructions implementing read channel functionality (page 485, do_rdwt function).

15. Claims 1 – 4 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Hunaker (US Patent Application Pub. No. 2003/0036198).

16. With respect to claim 1, Hunsaker discloses a computing system (figure 1) comprising:

a processor having a data/control bus interface (processor 110);

a data/control bus (host bus 120) implementing one or more device communication channels;

a data memory (system memory 140) coupled to the processor;

a mass storage device (hard drive,176, floppy, 174, and CD ROM 172) having an interface for communicating mass storage transactions; and

a controller (memory controller hub 130, or alternatively, MHC 130 and ICH 150) having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface and operable to conduct mass storage transactions between the data memory and the mass storage device.

17. With respect to claim 2, the data memory is coupled to the processor by a memory bus (system memory 140 is coupled to the processor via its own memory bus through the controller 130) operating independent of the data/control bus (the host bus 120 and the unlabeled memory bus are independent buses). The Examiner notes that the only configuration where there are two

busses directly coupled to the processor is the one shown in figure 6. However this configuration does not meet the controller requirements of claim 1.

18. With respect to claim 3, the controller comprises a memory access controller coupled to the processor, the data memory, and the mass storage device and operable to arbitrate accesses to the data memory between the mass storage and the processor (the controller MHC 130 controls access to the system memory and is the nexus that connects all of the claimed elements).

19. With respect to claim 4, the controller comprises a direct memory access controller (page 2, paragraph 19) coupled to the data/control bus, wherein the mass storage interface comprises a logical connection formed using one of the device communication channels.

20. With respect to claim 21, the mass storage device comprises an optical storage device (CD ROM 172).

21. Claims 1, 12, 13 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Zaidi *et al.* (US Patent No. 6,601,126, hereinafter "Zaidi").

22. With respect to claim 1, Zaidi discloses a computing system (figure 28) comprising:

a processor having a data/control bus interface(CPU);

a data/control bus (CPU bus) implementing one or more device communication channels;

a data memory coupled to the processor (DRAM);

a mass storage device (DMA peripheral, see col. 27, lines 41 – 45) having an interface for communicating mass storage transactions; and

a controller (bridge and MAC) having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface and operable to conduct mass storage transactions between the data memory and the mass storage device.

23. With respect to claim 12, (figure 1, and col. 4, lines 27 – 46, figure 28 is one of the embodiments of this system on chip) the controller is integrated with the processor on a single integrated circuit chip.

24. With respect to claim 13, the mass storage device's interface comprises a peripheral component interconnect (PCI) standard-compliant interface (figure 28).

25. With respect to claim 20, the computing device comprises a network appliance (col. 27, lines 40 – 45, in a networking application one of the DMA peripherals would be a network controller) having a network controller coupled to the data/control bus.

26. Claims 1, 14 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriarty *et al.* (US Patent No. 6,128,669, hereinafter "Moriarty").

27. With respect to claims 1 and 14, Moriarty discloses a computing system (figure 1) comprising:

a processor having a data/control bus interface(100);

a data/control bus (102) implementing one or more device communication channels;

a data memory coupled to the processor (104, or alternatively 112);

a mass storage device (144) having an interface for communicating mass storage transactions; and

a controller (106, or alternatively 106 and 108) having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface and operable to conduct mass storage transactions between the data memory and the mass storage device.

28. With respect to claim 20, computing device comprises a network appliance having a network controller coupled to the data/control bus (network controller 128 is coupled to 102 through 106).

29. Claims 1, 13 – 16, and 20 – 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Yiu *et al.* (US Patent Application Pub. No. 2003/0181205, hereinafter "Yiu").

Yiu discloses a computing system (figure 3) comprising:

a processor having a data/control bus interface(31);

a data/control bus (41) implementing one or more device communication channels;

a data memory coupled to the processor (33);

a mass storage device (34) having an interface for communicating mass storage transactions; and

a controller (page 3, paragraph 34) having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface and operable to conduct mass storage transactions between the data memory and the mass storage device.

Yiu discloses various interfaces claimed in claims 13 – 16 (page 3, paragraph 34), and mass storage types claimed in claims 21 – 22 (page 3, paragraph 35). A network controller of claim 20 is disclose as well (figure 3,37 – 38, page 3, paragraph 36)

30. Claims 1 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ellison *et al.* (US Patent Application Pub. No. 2002/0144121, hereinafter "Ellison").

Ellison discloses a computing system (figure 1C) comprising:

a processor having a data/control bus interface (processor 110);

a data/control bus (host bus 120) implementing one or more device communication channels;

a data memory (system memory 140) coupled to the processor;

a mass storage device (hard drive,176, floppy, 174, and CD ROM 172) having an interface for communicating mass storage transactions; and

a controller (memory controller hub 130, or alternatively, MHC 130 and ICH 150) having a memory interface coupled to the data memory and a mass storage interface coupled to the

mass storage device's interface and operable to conduct mass storage transactions between the data memory and the mass storage device.

The computing device comprises a set-top box including processes for implementing audio/video behaviors in the processor (page 1, paragraph 13).

31. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Houston *et al.* (US Patent No. 6,493,656, hereinafter "Houston").

Houston discloses a computing system (figure 1) comprising:

a processor (100) having a data/control bus interface;

a data/control bus (104) implementing one or more device communication channels;

a data memory (106) coupled to the processor;

a mass storage device (118, 122) having an interface for communicating mass storage transactions; and

a controller (102, or 102 and 114, or 102 and 121) having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface and operable to conduct mass storage transactions between the data memory and the mass storage device.

wherein the mass storage device comprises:

a spinning disk having magnetic storage media provided on at least one surface;

a head for accessing data stored in the magnetic storage media;

an actuator mechanism for moving the head relative to the magnetic storage media in response to commands (col. 1, lines 37 – 52);

a servo controller coupled to receive requests transferred from the data memory by the controller and generate the commands to the actuator mechanism (figure 2).

Conclusion

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
June 7, 2004

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